CLAIMS

Please amend the claims as follows:

18. (canceled)

19. (canceled)

20. (original) ~~The~~ A network chip for a node in a system area network including a plurality of nodes ~~of Claim 19~~, said network chip comprising:

a port for inter-node communication;

means for marking the port to prevent transmission to another node of packets of a first traffic type while permitting transmission to another node of packets of a second traffic type, wherein said means for marking comprises means for marking said port by setting a port configuration register;

a routing table that associates said port with a node identifier of at least one of said plurality of nodes; and

means for, if said port is marked, routing via said port only packets not of said first traffic type, wherein said means for routing routes packets by reference to said routing table.

21. (amended) The network of Claim [[18]] 20, wherein said network chip comprises means for determining a traffic type of a packet by reference to a packet header of the packet.

22. (canceled)

23. (amended) ~~The~~ A network chip for a node in a system area network including a plurality of nodes ~~of Claim 22, and further comprising~~, said network chip comprising:

a port for inter-node communication;

means for marking the port to prevent transmission to another node of packets of a first traffic type while permitting transmission to another node of packets of a second traffic type, wherein said first traffic type comprises non-configuration traffic and said second traffic type comprises configuration traffic;

means for, if said port is marked, routing via said port only packets not of said first traffic type; and

means for, following transmission of packets of configuration traffic, removing said marking of said port.

24. (amended) The network chip of Claim 23, and further comprising means, responsive to transmission of said packets of configuration traffic, for altering a node identifier used in packet routing.

25. (amended) ~~The~~ A network chip for a node in a system area network including a plurality of nodes ~~of Claim 18~~, said network chip comprising:

a port for inter-node communication;

means for marking the port to prevent transmission to another node of packets of a first traffic type while permitting transmission to another node of packets of a second traffic type, wherein said means for marking comprises means for automatically marking said port if said port is unconnected at initialization of the system area network; and

means for, if said port is marked, routing via said port only packets not of said first traffic type.

26. (newly entered) A node for a system area network including a plurality of nodes, said node comprising:

a processor;

a memory coupled to said processor; and

a network chip in accordance with Claim 20 coupled to said processor.

27. (newly entered) A system area network, comprising:

a plurality of nodes; and

a network coupling said plurality of nodes for communication;

wherein a node among said plurality of nodes includes a network chip in accordance with Claim 20.

28. (newly entered) A node for a system area network including a plurality of nodes, said node comprising:

a processor;

a memory coupled to said processor; and

a network chip in accordance with Claim 23 coupled to said processor.

29. (newly entered) A system area network, comprising:

a plurality of nodes; and

a network coupling said plurality of nodes for communication;

wherein a node among said plurality of nodes includes a network chip in accordance with Claim 23.

30. (newly entered) A node for a system area network including a plurality of nodes, said node comprising:

a processor;

a memory coupled to said processor; and

a network chip in accordance with Claim 25 coupled to said processor.

31. (newly entered) A system area network, comprising:

a plurality of nodes; and

a network coupling said plurality of nodes for communication;

wherein a node among said plurality of nodes includes a network chip in accordance with Claim 25.